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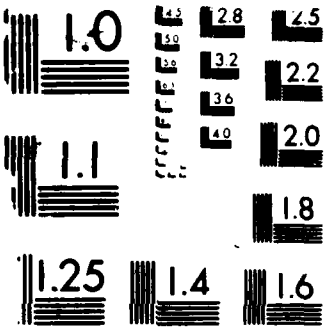

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This research program investigates the effect of extreme submicron spatial modulation of the electrostatic potential on the transport of electrons in silicon and in III-V compound semiconductor devices. The test vehicle is the so-called grating-gate FET (GGFET). When made to move in a direction perpendicular to the potential modulation, i.e., perpendicular to the grating gate, electrons experience a surface superlattice (SSL) effect. When moving along the potential modulation electrons are restricted to only one degree of freedom and thus constitute a one-dimensional system.

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The major accomplishments to date are in process technology and design of the devices. They are: (1) Double X-ray/deep-UV exposure of PMMA to simultaneously define fine and coarse patterns; (2) High temperature (950 °C) anneal of Si wafer after delineation of tungsten conductor patterns, to eliminate x-ray damage of silicon dioxide; and (3) Design of GaAlAs/GaAlAs structure for the implementation of the III-V GGFET.

Report No. AFOSR-85-0376-001

STUDY OF QUANTUM MECHANICAL EFFECTS IN DEEP SUBMICRON, GRATING-GATE FIELD EFFECT TRANSISTORS

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STUDY OF QUANTUM MECHANICAL EFFECTS IN DEEP SUBMICRON, GRATING-GATE FIELD EFFECT TRANSISTORS

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Annual Progress Report
September 30, 1985 through September 29, 1986

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This research program investigates the effect of extreme submicron spatial modulation of the electrostatic potential on the transport of electrons in silicon and in III-V compound semiconductor devices. The test vehicle is the so-called grating-gate FET (GGFET). When made to move in a direction perpendicular to the potential modulation, i.e., perpendicular to the grating gate, electrons experience a surface superlattice (SSL) effect. When moving along the potential modulation electrons are restricted to only one degree of freedom and thus constitute a one-dimensional system.

To date we have concentrated our effort on the fabrication of the silicon and III-V GGFET devices. Our progress is described below.

A. Silicon GGFETs

Our efforts over the past year have focused on understanding and solving the problems encountered during previous attempts to fabricate the surface superlattice (SSL) and quasi-one-dimensional (Q1D) grating-gate field effect transistor (GGFET). This understanding has evolved to the point where we feel the GGFET can be made with yields as high as conventional MOSFET devices. Reliable fabrication of the GGFET will permit unique experiments in the basic physics of electronic conduction in macroscopic phase-coherent quantum systems. The primary feature which distinguishes the SSL GGFET from other superlattices, such as those fabricated using molecular beam epitaxy, is that the strength of the periodic modulation can be controlled with a voltage supply. In sharp contrast to systems attempting to emulate static crystal properites, the SSL GGFET functions as a voltage controlled "crystal". The feature distinguishing the Q1D GGFET from other structures designed to study Q1D inversion layers is its relative insensitivity to the sample-specific fluctuations characteristic to those of other structures. This feature is due

to the averaging effect resulting from placing a very large number of Q1D channels in parallel.

The GGFET is a dual stacked-gate MOS-type structure in which the gate closest to the inversion layer is a very fine period grating made of a refractory metal. A silicon dioxide insulating layer separates a continuous aluminum upper gate from the grating gate and the inversion layer. This dual stacked gate structure is very advantageous for experiments involving both the SSL and Q1D GGFET. In the case of the SSL, the dual gate allows independent control of the average electron density in the inversion layer and of the strength of the periodic modulation. In Q1D devices the dual gate allows the formation of inversion strips between gate wires. This permits easy control of the inversion layer width.

The dual stacked-gate structure giving the GGFET experimental advantages also gives rise to many problems associated with its incorporation into conventional MOS transistors. Problems encountered in previous attempts to fabricate the GGFET include (1) poor electrical contact to the grating gate; (2) shorting from the grating gate contacts to the silicon substrate; (3) inability of the refractory metal to withstand high temperature anneal without oxidizing. X-ray lithography and electron beam metal deposition techniques used to make the grating gate result in significant radiation damage to the silicon dioxide insulating layer between the grating gate and the inversion layer. The annealing step is thus crucial to fabricating GGFETs with high electron mobility.

We have solved these problems as follows: (1) by using the industry standard local oxidation of silicon (LOCOS) process as opposed to the previous planar device process; (2) by developing a deep-UV lithography system to double-expose PMMA, thus allowing simultaneous formation of the grating gate contacts and of the grating by a single electron beam evaporation of the refractory metal; and (3) by finding a capping material which prevents oxidation of refractory metal grating lines during the high temperature anneal.

To prevent the grating gate contact pads from shorting to the substrate, it is desirable to place the contact pads over a thick silicon dioxide layer. This necessitates the implementation of a nonplanar device geometry. The LOCOS MOSFET device geometry is ideal because of the gradual transition from the thin gate oxide to a thick field oxide. Grating lines formed on the LOCOS geometry were shown by inspection in the scanning electron microscope to be continuous over the transition region known as the bird's beak. We also designed a new mask set to implement this process.

In previous attempts to fabricate the GGFET contact to the grating gate was unreliable because of the native oxide barrier formed between the grating wires after their deposition and the subsequently deposited contact pads. The uneven surface of the contact pads deposited directly on top of grating wires also resulted in cracks and poor adhesion of the pads. In previous attempts

to fabricate GGFET these pads peeled off the grating wires. Both problems contributed to shorting between the pad and substrate during subsequent etching through the upper gate oxide needed to contact the pad. To solve this problem we have developed a deep-UV lithography system to expose gross features in PMMA prior to x-ray exposure of the grating wires. Exposure times were tailored such that the contact pads and grating wires developed simultaneously in PMMA. Subsequent e-beam evaporation of a refractory metal and its capping material form the grating wires and their contact pads simultaneously. The contact pads now adhere well to the substrate and are free of breaks or discontinuities. They act as a reliable etch stop in subsequent device processing.

A high temperature (950 ^{o}C) step is necessary to anneal radiation damage of the gate oxide caused by x-ray lithography and e-beam metal evaporation. Refractory metals oxidize above 200 ^{o}C by reacting with oxygen in CVD silicon dioxide. To prevent the grating gate metal from oxidizing, we deposited a capping material on top of the metal to act as a diffusion barrier to oxygen. We also built a furnace tube insert which can be pumped down to permit vacuum annealing at high temperature. This prevents the small amount of oxygen which is present in a regular furnace from reaching the wafer. With a combination of a capping layer and vacuum annealing, we have proven that the grating gate metal does not significantly oxidize during annealing.

At this point we have put together all of the previously discussed processing improvements into a new fabrication sequence for GGFETs. We expect to have working devices early in 1987. If everything goes well, device measurement and characterization will start in January of 1987.

B. III-V GGFETs

Within the last few years, the subject of electronic transport in quantum confined systems has become one of the hottest topics in condensed matter physics. The silicon GGFET device has exhibited reproducible "structure" in the drain current (and transconductance) gate voltage curves at liquid helium temperatures. This structure was attributed to the "mini-gaps" in the energy band diagram caused by the additional periodic potential of the gate metal. As the gate voltage is modulated, the Fermi level of the inversion layer electrons is swept past these mini-gaps, causing fluctuations in the conductivity and, hence, to the drain current. Since the mobility of silicon is low, the electrons do not travel much more than 0.2 μm at a few degrees Kelvin before suffering an inelastic collision, thereby losing phase coherence. For an electron to truly feel the effect of a periodic gate potential it must travel at least several grating periods between inelastic scattering events. We do know, however, that high electron mobility devices (HEMT) can achieve high mobility (i.e., longer mean free path) even at room temperature. If indeed these quantum effects are inherent in such surface superlattice devices, then the effect observed in a Si GGFET at 1.2 K should

appear in the characteristics of a HEM-GGFET at 77 K, due to the substantially higher mobility of the latter device.

To get a better understanding of the HEMT, which is the basic block in building surface superlattices on III-V compound materials, the device is simulated in the semiclassical limit. Many of the effects we anticipate from our HEM-GGFETs (e.g., Block oscillations, quantum tunneling, etc.) have to be simulated in the quantum regime. Nevertheless, a semiclassical simulation of the HEMT based on the solution of Boltzmann's transport equation is very helpful to get the right design of the device, i.e., the required thickness of layers and doping levels.

In our device simulator we are solving simultaneously the following four equations for electrons: (1) Electron conservation, (2) Energy balance, (3) Momentum, and (4) Poissons equation. These equations account for the conduction band discontinuity ΔE_c, for the density of state difference, and for a change in the dielectric constant from one medium to another. Simulation results show that for an $Al_{0.3}Ga_{0.7}As$ layer with a doping level of 10^{18} cm^{-3}, its thickness has to be 375 Å to prevent parallel conduction on one hand and to get an appreciable amount of carriers in the two-dimensional gas on the other. This amount is calculated to be 8.5×10^{11} cm^{-2} at zero gate bias. If a slightly negative bias is applied to the gate, the charge concentration in the two-dimensional gas is reduced. Thus, in the case of a grating gate, we expect the charge concentration along the two-dimensional gas to be modulated by the existence of the periodic gate. The periodicity will be the same as for the gratings, but with a slight smearing due to the fringing fields. This modulation effect was checked by simulating a HEMT with two 0.1 μm gates separated by 0.1 μm. The simulation is also exploited to study the possibility of making use of the HEM-GGFET structures as tunable microwave oscillators. This is mainly based on the negative differential mobility available in GaAs leading to charge packet formation and movement under certain conditions.

The process for fabricating the HEM-GGFET has been tailored so that it contains the fewest number of steps possible. The process is as follows:

1. The standard HEMT layers are grown by MBE on a p^+ [$\geq 10^{18}$ cm^{-3}] GaAs substrate. First a nominally p-type GaAs[10^{14} cm^{-3}] layer is grown. Then a n^+ $Al_{0.3}Ga_{0.7}As$ [10^{18} cm^{-3}] layer is grown, and finally, an n^+ GaAs [5×10^{18} cm^{-3}] layer is grown on top.

2. Ge and Au films for ohmic contacts are evaporated.

3. A sacrificial oxide is sputtered on top of the Au/Ge film.

4. The active channel is defined by standard lithography, reactive ion etching the oxide, ion milling the Au and Ge, and wet etching the GaAs.

5. The ohmic contact metal is alloyed.

6. PMMA is spin-coated over the surface and exposed to deep-UV radiation to define the large gate contact pads. Then the sample is exposed by X-ray lithography to make the gratings. The PMMA is then developed.

7. Ti, Pt, and Au are evaporated in that order to form the Schottky barrier gate, and the rest of the metal is lifted-off. Note that the combined deep-UV and X-ray step enables us to define the gratings and the gate contact pads with one lift-off step.

8. Grating lines are removed from everywhere except from the channel by wet etching. The oxide is then etched away.

9. Source and drain pads are defined by a lithography step which covers the source/drain/active channel area. The uncovered metal is ion milled away.

10. Individual devices are isolated by mesa etching.

As the queue for MBE-grown layers is quite long, it pays to be sure that all the process steps are well understood and repeatable on Si test wafers before proceeding to GaAs HEMT layers. We have concluded tests of all of the listed process sequences. At this point we have: (1) designed the mask set for the devices using the in-house CAD system; (2) measured the ion milling rate of Au and Ge; (3) measured the etch rate of sputtered oxide in CHF_3 (reactive ion etched); and (4) developed the capability of combining deep-UV and X-ray lithography to make metal lines which run directly into a continuous metal gate pad. We have now finished the testing, and the GaAs wafers with the HEMT layers are being processed. When these devices are completed, measurements will be taken at room temperature, at 77 K, and ultimately at liquid helium temperature.

Working on this particular device has spawned new ideas for future generations of these surface superlattice devices. We have completed the design of a new mask set which will enable us to make, on the same chip, surface superlattice HEMTs with two different channel lengths and a 1 μm channel length continuous gate (conventional) HEMT. By looking at the device characteristics, we could compare our HEMT process with the standard HEMT process which uses liftoff to define source and drain. Also, we plan to fabricate a device with a crossed grating gate, or a surface superlattice grid, which would allow us to look at the transport properties of a two-dimensional bounded electron gas. We expect the first HEM-GGFET devices to be completed by February of 1987.

END

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